AMIYA PRASAD BEHERA

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Career Objective

I intend to build my career as a successful professional, working in a creative and challenging environment, which will provide me the scope to explore my potentials and responsibilities to contribute to the growth of the corporate and myself as well.

Professional Profile

6.5+ Yrs of industry experience with focus on Analog Design and Layout at Sankalp Semiconductor Pvt. Ltd from July 2008 till date.

Had 1 year of working experience with Texas Instruments India (TII) in ODC/ Embassy model and 7 months of on-site working experience with ST Micro-electronics, GNoida, as a contractor from Sankalp Semiconductor Pvt. Ltd.

Educational Qualification

Bachelor of Technology in Electronics and Instrumentation Engineering from National Institute of Science and Technology, Berhampur, Orissa with CGPA of 8.89.

Professional Experience

- 3 months of Analog and Mixed Signal Layout training from Sankalp Semiconductor Pvt. Ltd.
- Layout of multiple bias blocks, amplifiers, comparators, reference generators, non-overlapping clock generator, high speed MIPI_DPHY transmitter and receiver, clock generator modules for wireless applications
- Design of Programmable Frequency Dividers, PFD, Lock Detector, Calibration, CML2CMOS logic, Reference buffers and bias blocks, Non-overlapping clock generators, Rail-to-Rail OTA, Wide range CMOS VCOs, Brown-out Detector, PLL loop modelling and loop filter design, Precision sine wave oscillator, LVDT modelling etc.
- Design of multiple PLLs and Frequency Synthesizers with frequency ranging from 6.4GHz to 500MHz and with different architectures and programmability.
- Regression of tool AnXplorer from Ago Inc.
- Development of Sankalp in-house tool Nimble, a substitute for Analog Design Environment, compatible with Spectre, Eldo and AFS simulators
- Driving multiple Analog Design Automation activities in Sankalp Semiconductor Pvt. Ltd.
- Development of VPS EM Check Wrapper for Texas Instruments, Dallas, USA
- Worked in multiple technology nodes, like 180n, 130n, 110n, 90nm, 65n, 45nm and 28nm from foundries like TMSC, IBM, UMC, GSMC and GPDK.

Project Details

- **Design of 500MHz to 1GHz VCO PLL with free running VCO**
  - **Description**: Design and verification of 500MHz to 1GHz PLL having free running VCO to improve lock time. Design in IMG140nm technology with supply range from 1V to 1.35V using EldoD simulator.
  - **Responsibilities**:
    - Design of the free-running circuit for VCO along with the V2I splitter.
    - Design of other analog blocks and verification of PLL Top.
  - **Challenges**:
    - Minimizing the frequency jump during the transition from free-running mode to active mode of PLL.
    - Circuit to isolate the VCO from band-gap noise current in PLL active mode
- **2GHz VCO programmable PLL with wide reference frequency range**
  - **Description**: Design and verification of 1GHz to 2GHz in CMOSM40 40nm technology with a supply range of 1.05V to 1.3V. PLL input frequency ranging from 8MHz to 50MHz.
  - **Responsibilities**:
    - Implementation of splitter in LF and VCO V2I to reduce area.
    - Design and verification of the analog blocks of the PLL. PLL Top Level simulation on both Pre- and Post- Layout Netlists.
  - **Challenges**:
    - Use of splitter in V2I, Duty-cycle correction of VCO buffer, balancing between CPUMP gain and SPE
- **Fast Locked Loop based high frequency PLL design**
  - **Description**: Design of FLL (Fast Lock Loop) based PLL architecture, where PLL locks in 250cycles of reference clock. Design of VCO having both thermometric as well as SAR DAC based V2I converter. Design of two PLLs with frequency 3.2GHz - 6.4GHz and 2GHz - 4GHz in 28nm FDSOI process at a typical supply of 1.8V
  - **Responsibilities**:
    - Design of FLL bias based VCO, Verification of FLL
    - Design and verification of other analog blocks of PLL along with Top-Level verification
    - Implementation of splitter in LF and VCO V2I to reduce area.
  - **Challenges**:
    - Development of the unique V2I structure, Duty-cycle correction of VCO buffer, trade-off between VCO frequency and analog current
    - Meeting fine lock-timing specification of 250 cycles of input frequency

- **Porting of 1.4GHz PLL from 90nm GP to LP Process Technology**
  - **Description**: Porting of 700MHz-1400MHz VCO PLL, having Normal, Fractional and SSCG Mode of operation from 90nm GP to 90nm LP process. Two quadrature phase shifted outputs with programmable Charge-Pump architecture with dual VCO supply range (AVDD : 2.5V and DVDD : 1.8V)
  - **Responsibilities**:
    - Design and verification of analog blocks of PLL along with Top-Level pre- and post-layout verifications.
  - **Challenges**:
    - Duty-cycle correction of VCO buffer, trade-off between VCO frequency and analog current
    - Designing the programmable CPUMP and achieving gain error close to unity with lesser Static Phase Error
- **Development of VPS EM Check Wrapper for TI Dallas, USA**
  - **Description**: VPS Electro-Migration check flow consists of steps like LVS, layout extraction, test-bench creation, post extraction simulation and Power EM analysis. To make the EM check flow easier, the wrapper is developed. Wrapper runs all the analysis in batch mode, either in XTerm or as LSF jobs.
  - **Responsibilities**:
    - Doing feasibility check for multiple methods of EM check, like full-chip, single/multiple cell, single/multiple instances, all instances of hierarchy, power-plot based and abstract view based EM check.
    - Implementation of the wrapper for different methods.
  - **Challenges**:
    - Getting used to the batch mode commands and scripting languages.
    - Handling the huge simulation result file and extracting bias information, test-bench creation.
    - Getting the required layout ready for use in the wrapper flow, where the layout was not done with full standards.
    - Getting a LVS clean layout abstract view
- **Brown Out Detector (BOD) with Programmable Threshold**
  - **Description**: The programmable BOD circuit has 8 threshold levels ranging from 1.7V to 4.3V with a 5.5V supply. BOD generates a logic high pulse, when the supply spike remains below threshold for longer than 300ns. Design Technology/Process Node: 180nm GSMC ULL CMOS Technology
  - **Responsibilities**: Circuit design and simulation of BOD
  - **Challenges**:
    - Design of resistor divider and implementation of hysteresis in it
    - Minimizing power consumption and meeting the threshold band

- **High precision sine wave oscillator for LVDT application**
  - **Description**: The high precision sine wave oscillator has oscillation frequency of 3128Hz. The oscillation output amplitude and frequency stability has to be within ±0.5%. The design expects an SNDR of at least 60dB for a supply voltage of 3 Volts with minimal off-chip components. Design Technology/Process Node: 65nm TSMC LP CMOS Technology
  - **Responsibilities**:
    - Different oscillator architecture evaluation and selecting the best suitable
    - Circuit design and simulation of sine wave oscillator circuits along with AGC circuits and error correction scheme
  - **Challenges**:
    - Design of amplitude stabilization circuit and accurate full-wave rectifier
    - Meeting the design specification for SNDR and amplitude and frequency stability
    - Process and temperature compensation of Oscillation amplitude and frequency.
- **Evaluation of Ago Tool**
  - **Description**: Ago Anxplorer is a design optimization tool developed by Ago Inc. It finds out the optimum design points that match the given design constraints. Other features include finding out the variation in output using sensitivity analysis, design porting optimization. Design Technology/Process Node : 65nm TSMC LP CMOS Technology
  - **Responsibilities**: Evaluation of the tool with respect to analog and high frequency circuit design and reporting the bugs to the developers
  - **Challenges**: Understanding the tool flow, setting the design space of design variables and specifying the design constraints for different analysis that need to be performed
- **6 Phase Wide Range VCO with rail-to-rail OTA**
  - **Description**: The wide range VCO has a linear frequency range of 1GHz to 4GHz, with K_{VCO} range of 3.5GHz/V to 11.5GHz/V for a core supply voltage of 1.2V. Design Technology/Process Node : 65nm TSMC LP CMOS Technology
  - **Responsibilities**:
    - Design of a wide range 3 stage ring oscillator, a linear rail to rail voltage to current generator and there integration
    - Process and temperature compensation of VCO.
  - **Challenges**:
    - Meeting the required linear frequency range for ring oscillator
    - Design of a linear rail-to-rail V2I converter for a control voltage of 300mV to 900mV

- Keeping the V2I converting MOS in linear region across PVT and its temperature compensation.
- Meeting the design specification for K_{VCO} and phase noise of VCO

- **4 Phase Wide Range VCO with rail-to-rail OTA**
  - **Description**: The wide range VCO has a linear frequency range of 1GHz to 2.8GHz, with K_{VCO} range of 1GHz/V to 5.2GHz/V. The linear rail to rail V2I converter has a novel temperature compensation scheme as well as a novel curvature compensation scheme. Design Technology/Process Node : 65nm UMC SP CMOS Technology
  - **Responsibilities**:
    - Design of a wide range 2 stage differential ring oscillator, a linear rail to rail voltage to current generator and there integration
    - Process and temperature compensation of VCO.
  - **Challenges**:
    - Meeting the required linear frequency range for ring oscillator with minimal power
    - Design of a linear rail-to-rail V2I converter for a control voltage of 300mV to 1.35V for a regulated supply voltage of 1.65V
    - Biasing of V2I MOSFET, Curvature compensation of the rail to rail current near threshold voltages and temperature compensation of the linear current using sub-threshold MOS current
- **Nimble Development and Up-gradations**
  - **Description**: Nimble is a Sankalp in-house developed tool for designers. The tool is written using skill and shell scripts. Some portion of the tool uses Ocean and Perl also. Up-gradation of Nimble with time, starting with version 2.0 to 4.4.
  - **Responsibilities**:
    - To set proper flow of the tool and improvement in the look of the form. To add multiple analysis syntaxes, fixing multiple bugs, adding multiple functionalities to the tool, like setting initial condition, bug reporting etc.
    - Introduction of corner concept in parametric analysis and post processing of simulation data. Multiple new features are added to the tool in recent upgrades.
    - Including multiple circuit simulator options to the tool
  - **Challenges**:
    - Understanding the scripting language, file processing and the old source code.
    - Preparing the windows for best view in both Virtuoso and ICFB.
- **Design of CDR for HDMI Applications**
  - **Description**: Design and simulation of multiple blocks of CDR module, such as feedback divider (Programmable), Reference divider, Lock detector and CML2CMOS circuits. The CDR module works in 3 different modes: hdmi, dp and dp-like-hdmi. Design Technology/Process Node: 45nm TSMC LP CMOS

- **Responsibilities**: Circuit design and simulation of dividers, lock detector and CML2CMOS circuits in all 3 different modes of operation.
- **Challenges**:
  - Design of high frequency, differential frequency divider and meeting the specification for clock frequency of 3.5GHz
  - Meeting timing of lock detector for 3 different modes of CDR operation
  - Meeting the Gain and Bandwidth specification along with proper output common mode and PSRR number for CML2CMOS. Meeting the amplitude and frequency specification of 60mV and 3.5GBPS for CML2CMOS.

- **Design of HDTX and HDRX for HDMI Applications**
  - **Description**: Design and simulation of multiple blocks of HDTX and HDRX modules, such as Programmable feedback divider, VCO Calibration and CML2CMOS circuits. Design Technology/ Process Node : 65nm TSMC LP CMOS Technology
  - **Responsibilities**:
    - Circuit design and simulation of 3.5GHz Programmable frequency divider and VCO calibration block for PLL.
    - Circuit design of CML2CMOS block for 3.5GBPS data rate with a minimum input peak to peak voltage of 70mV and maximum input of 400mV
  - **Challenges**:
    - Design of high frequency, differential frequency divider and meeting the design specification
    - Meeting the Gain and Bandwidth specification along with proper output common mode and PSRR number for CML2CMOS along with the amplitude and frequency specification of 70mV and 3.5GBPS.

- **Layout of Clock Generator Modules for WCS-18XX**
  - **Description**: Layout of clock generator modules that generates clocks for FM, BT, GPS, NFC and WLAN modules. Layout of top level CLKM_18XX modules consisting of 1 Lane and 2 Lane clock generators (primary and secondary clock divider sections) except Bond Pad. Technology/ Process Node : 65nm TSMC CMOS Technology
  - **Responsibilities**:
    - Layout of the clock generator module that generates multiple clocks with symmetric routing, Clock Dividers, MUX, Buffers, XOSC, SLICER and SLICER_BIAS blocks
    - Top-level layout of two CLKM_18XX modules, consisting of the above blocks along with LDOs, array of level shifters, IO cells and CDM Clamps
    - Ramping up of two assets in TI layout flow and enabling them to work in TI flow
  - **Challenges**:

- Meeting the symmetric routing of clocks in clock generator, routing resistance in clock lines as well as power lines, routing of reference voltage line across the module
- Top level layout of CLKM_1893 and CLKM_1853, except Bond PAD
- Working with Hercules verification tool for checks like DRC, LVS, Antenna, Nucleus and HV

- **Layout of DAC**
  - **Description**: Layout of Bias block and level shifter for DAC. Layout modification for multiple blocks has to be done. Top level layout modifications and verification (Hercules DRC, LVS, Antenna, Nucleus and HV). Technology : 65nm TSMC CMOS Technology
  - **Responsibilities**:
    - Capacitor unit cells characterization to find out post extraction capacitance value. Layout and verification of DAC_BIAS and level_shifter_DAC_TOP. Top level integration of DAC_BIAS and level_shifter_DAC_TOP
    - Layout modification of DAC_LSB_CELL_HEM, DAC_TOP and verification
  - **Challenges**: Meeting constraints like matching and resistance in power line, symmetric routing of matched signal line, Capacitor routing, Working with Hercules verification tool
- **Design of Reference buffers, Bias blocks, clock generator for ASDM ADC**
  - **Description**: Reference buffer provides two common mode voltages for the ASDM ADC stages and also references to comparator block. Bias blocks used to provide bias voltages to amplifiers. Non-overlapping clock generator provides four phase clock to the ASDM module. Design Technology/ Process Node : 65nm TSMC LP CMOS Technology
  - **Responsibilities**:
    - Both circuit design, layout and back annotation of multiple blocks
  - **Challenges**:
    - Generation of non-overlapping clocks
    - Meeting the bias margin for MOSFETs, having very high threshold voltage
    - Layout of clock generator, where both the outputs has to be symmetrically routed
- **Design of Programmable Frequency Dividers for PLL**
  - **Description**: Fractional frequency divider design for 2GHz and 800MHz PLL output frequency. Divider has fractional resolution of 156.25Khz for a reference clock frequency of 10MHz. Design Technology/ Process Node : IBM, UMC 65nm and 180nm Technology
  - **Responsibilities**:
    - Understanding the concepts of fractional frequency synthesizer

- Design of CMOS Digital logic gates, MUX, Latches, flip-flops and Level shifters
- Design of integer as well as fractional frequency dividers

➢ **Challenges**:

- To meet the critical path delay

- **Block level Layout of Amplifiers, ADC and Comparator**
  - ➢ **Description**: All the blocks has to be done in CMOS process with different technologies like 180nm and 130nm
  - ➢ **Responsibilities**: Floor planning of Blocks, Placement ,Routing & Verification
  - ➢ **Challenges**: Placement & Routing of blocks to meet constraints
- **MIPI HS Transmitter & Receiver, MIPI BGR & LDO**
  - ➢ **Description**: The Analog MIPI_DPHY is targeted to have two data lanes and a single clock. This analog chip is intended to dialogue with digital chip with third party MIPI interface at system level. Layout is done in 180nm technology.
  - ➢ **Responsibilities**: Floor planning, Placement and Routing of HSTX, HSRX, LPTX, LPRX, and LPCD
  - ➢ **Challenges**: Placement & Routing of blocks to meet matching, parasitic, EM & IR drop, ESD constraints on outputs
- **Blood Pressure Monitoring System**
  - ➢ **Description**: This was a training project. I had worked on Control Logic Module of BPM System. Design Technology/Process Node : GPDK 180nm CMOS Technology
  - ➢ **Responsibilities**: Design and Layout of the Control Unit, Top level routing & verification
  - ➢ **Challenges**: Meeting the timing constraints of different signals, Design of the synchronous digital control logic. Layout of offset amplifier and area optimization

Other Details

- **Automations**
  - ➢ License sharing tool for efficient use of licenses. Quality check codes for Assura verification. Multiple skill codes to increase efficiency of layout engineers.
  - ➢ Power plot in Laker using tcl and shell script.
- **Expertise in Tools**
  - ➢ Virtuoso Schematic, Layout L/XL Editor, ADE-L/XL, Spectre Simulator
  - ➢ Assura verification flow (DRC/LVS/RCX), Hercules verification (DRC/LVS)
  - ➢ Laker ADP, Laker L2/L3, Tanner EDA : S-edit, L-edit, T-spice and W-edit
  - ➢ Other Tools : IC-STUDIO, DAIC, EZ-Wave, ELDO Simulator
- **Modeling / Programming Languages**

- VHDL, Verilog, Verilog-A
- Skill, Perl, Shell, Python

- **Operating Systems Hands-On**
  - Linux and Windows

Conference Papers

- Paper on "Wide Range CMOS VCO for PLL Application" is presented on VLSID2013 and published under IEEE.
- Paper on "High precision sine wave oscillator for LVDT applications" is presented in Sankalp Technical Conference, 2012.

Hobbies

- Chatting with friends and net surfing.
- Watching TV

Declaration

I, hereby declare that the above statements made are complete and true to my knowledge and belief.

Date :
Place : (Amiya Prasad Behera)